

## Numerical simulations of contact resistance in organic thin-film transistors

I. G. Hill

Department of Physics, Dalhousie University, Halifax, Nova Scotia, Canada

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The origin of the source/drain contact resistance reported in studies of pentacene-based organic thin-film transistors (OTFTs) has been investigated using numerical device simulations. Quantitative agreement with published contact resistance values is obtained, using reasonable values for the physical parameters describing both the semiconductor material and the metal/organic interfaces. In particular, the difference in contact resistance measured in top and bottom contact OTFTs has been reproduced. © 2005 American Institute of Physics. [DOI: 10.1063/1.2112189]

Organic thin-film transistors (OTFTs) have yet to reach the early stages of commercialization, unlike organic light emitting devices (OLEDs). Nevertheless, the performance of pentacene OTFTs, in particular, rivals that of *a*-Si TFTs, which are the basis of the multi-billion dollar active matrix liquid crystal display (AM-LCD) industry. Already, prototypes such as a flexible, video rate, OTFT-based AM-LCD constructed on a polyethylene terephthalate (PET) plastic have been demonstrated.<sup>1</sup>

Despite these early successes, issues still exist which may limit the future use of OTFT technologies. For instance, relatively large source/drain contact resistance has been noted in the literature.<sup>2-4</sup> The reported contact resistance is large enough to render the devices too slow for use in high resolution displays, due to their inability to charge either a capacitive AM-LCD cell, or the gate capacitance of a drive transistor in an active matrix OLED pixel, in the required time (which scales as  $1/\#$  of rows in the display). Furthermore, the “bottom contact” geometry (Fig. 1), which is more amenable to photolithographic fabrication, is known to have a significantly higher contact resistance than “top contact” devices.

To better understand the experimental OTFT data produced in the laboratory, as well as those available in the literature, a well-established physical device simulation package, Stanford PISCES B.9009,<sup>5</sup> has been used to model OTFTs and better understand the contact resistance. PISCES is a two-dimensional physical device simulation package, originally designed for Si devices. As such, it is important to discuss the limitations of its application to organic molecular devices.

PISCES self-consistently solves the discrete Poisson and drift-diffusion equations on a user defined grid, subject to various semiconductor/contact boundary conditions, including Schottky contacts with image force barrier lowering, as were used in this study. The contacts are characterized by a work function, and the barrier lowering is calculated from the electric field at the contact and the relative permittivity of the semiconductor material.

In this work, the device geometry simulated was a cross section of a field effect transistor, where the 2-D simulation plane is perpendicular to the plane of the channel, and parallel to the direction of current flow in the channel (see Fig. 1). Simulated device currents are therefore extracted as linear current densities ( $A/\mu\text{m}$  of channel width). Actual device currents are calculated by simply multiplying the linear current density by the hypothetical channel width. Note that this

analysis assumes the channel width ( $W$ ) is much greater than the channel length ( $L$ ), as channel fringing effects are not simulated. This does not pose a problem, as laboratory OTFT devices usually meet this criterion.

Although originally intended for Si devices, PISCES allows user-defined semiconductor materials. The user defines parameters such as the room temperature band gap, the electron affinity, the electron and hole mobilities, effective densities of valance and conduction states, and relative permittivity of the semiconductor material. Many optional parameters, such as those describing the dependence of the band gap on temperature and various impact ionization models are also available, but were not used in this study. It is important to note that carrier mobilities in this study were assumed to be isotropic, which is known not to be the general case in organic semiconductor materials, where the mobilities may be strongly dependent on direction relative to

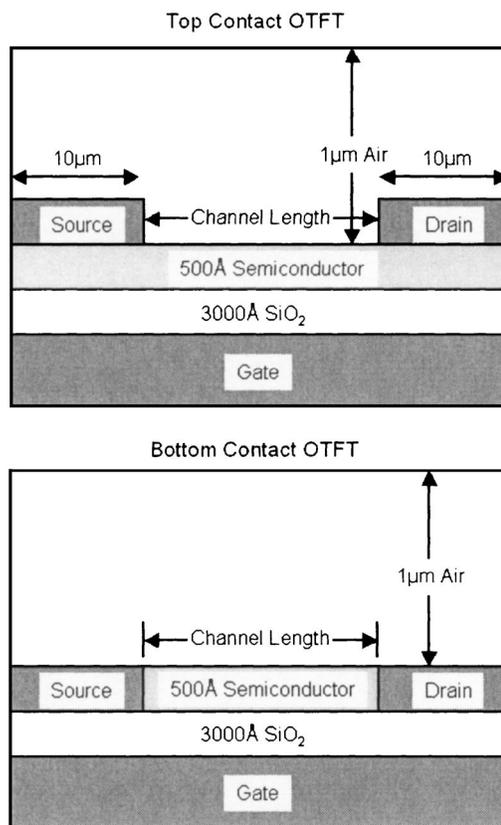


FIG. 1. The top and bottom contact OTFT devices used in the simulations.

crystalline planes.<sup>6</sup> The intention here is to compare simulated results with the results obtained from polycrystalline pentacene transistors, where the hole mobilities extracted from the data are the result of a macroscopic average of transport through crystalline grains with many different orientations, and through grain boundaries which have been suggested to be the bottle-neck for transport in these devices.<sup>7,8</sup> The assumption of an isotropic mobility is therefore safe, as long as the interpretation of the results is limited to macroscopic observables.

At this time, neither bulk semiconductor trap states nor semiconductor/dielectric interfacial trap states have been included in the simulations. This will not affect the interpretation of devices in the “on” state, but will affect parameters such as the on/off ratio, the threshold voltage and the sub-threshold slope. The discussion will therefore be limited to devices operating well into the linear and saturation regions. The presence of trap states also leads to gate field, or charge density, dependent carrier mobilities, as discussed in the literature.<sup>4</sup> This effect will therefore be absent in these simulations.

The device geometries simulated are presented in Fig. 1. Devices with 10  $\mu\text{m}$  wide top and bottom contacts were simulated in order to investigate the differences in contact resistance reported in the literature.<sup>2-4</sup> In each case, the hole mobility was assumed to be 1  $\text{cm}^2/\text{V s}$ . Reports of polycrystalline pentacene hole mobilities in the range of 0.3–3  $\text{cm}^2/\text{V s}$  are common in the literature [1-3, for example], and a value of 1  $\text{cm}^2/\text{V s}$  is considered typical. In this study, the OTFTs were modelled as hole-only devices. The dielectric was modelled as  $\text{SiO}_2$ , with a thickness of 3000  $\text{\AA}$  and a relative permittivity of 3.9. The band gap and electron affinity of the semiconductor were 1.85 and 3.15 eV, respectively, giving an ionization energy of 5 eV, which is consistent with parameters measured for pentacene using ultraviolet photoelectron spectroscopy (UPS).<sup>9,10</sup> The relative permittivity of the semiconductor was estimated to be 3, and the semiconductor thickness was set at 500  $\text{\AA}$ , which is consistent with typical pentacene devices in the literature. Transistor channel lengths of 1, 10, 100, and 1000  $\mu\text{m}$  were simulated. Many contact work functions were simulated, but the data presented here correspond to contacts having a hole injection barrier of 0.2 eV, as these most closely match reported data. The results correspond well with reported results of pentacene OTFTs using Pd source/drain electrodes.<sup>2,3</sup> This hole injection barrier is substantially lower than those measured for pentacene on Au (having a work function similar to Pd) using UPS: 0.55 eV (Ref. [9]) and 0.85 eV.<sup>10</sup> It has been noted, however, that the method of estimating hole injection barriers used in the analysis of organic semiconductor UPS data while sufficient for comparing UPS data for different metal/organic interfaces, systematically underestimates the effective barrier by a few tenths of an eV.<sup>11</sup> Thus, injection barriers of a few tenths of an eV are appropriate for modelling OTFTs with high work function metal source/drain contacts.

Simulated linear ( $V_s=0$  V,  $V_d=-2$  V,  $V_g=0\cdots-50$  V) and saturation ( $V_s=0$  V,  $V_d=-50$  V,  $V_g=0\cdots-50$  V) transfer curves were produced for each device. The data produced were analyzed as if it were experimental data—the maximum linear and saturation mobilities were extracted from the maximum slopes of the  $I-V_g$  and  $I-V_g^{1/2}$  curves, respectively. A summary of these data is presented in Fig. 2.

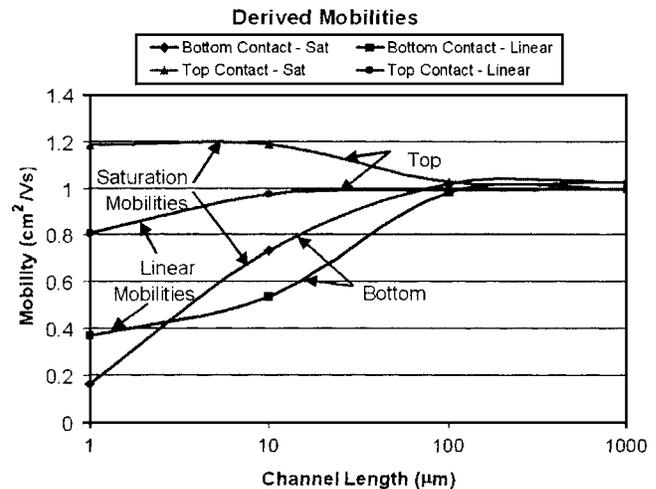


FIG. 2. Apparent hole mobilities extracted from the simulated data for a source/drain contact injection barrier of 0.2 eV and various channel lengths. Data are presented for both top and bottom contact geometries, in both the linear and saturation regions of operation.

In Fig. 2 several important observations are noted. At long channel lengths, the extracted mobilities agree well with the value input to the simulations (1  $\text{cm}^2/\text{V s}$ ), but at shorter channel lengths, the extracted mobilities deviate substantially from the input value. In the bottom contact geometry, below 100  $\mu\text{m}$ , both the linear and saturation mobilities are significantly lower than the input value. It is proposed that this is due to the higher contact resistance of the bottom contact geometry, as will be presented later. Contact resistance less affects long channel devices, because as the device is scaled to larger dimensions with a constant  $W/L$ , the total resistance due to the contact decreases as  $1/W$ , while the total current in the device remains constant.

For the top contact geometry, the apparent mobilities are less affected. The apparent top contact linear mobility is decreased by approximately 20% at a channel length of 1  $\mu\text{m}$ . The apparent top contact saturation mobility actually *increases* by about 20% for channel lengths  $\leq 10$   $\mu\text{m}$ . This is due to the well-known “short channel” effect in traditional FETs, channel length modulation. In the saturation region of operation, as the drain voltage approaches the gate voltage, the electric field is not strong enough to form an accumulation region near the drain contact. As a result, the effective channel is shorter than the actual distance between the source and drain electrodes. Since the device current varies as the product of the mobility and  $W/L$ , a decrease in the effective length,  $L$ , can appear as an apparently larger mobility. In short channel devices, the depleted region represents a larger fraction of the total channel length, and the effect becomes more pronounced. This effect was verified by examining the hole density in the channel as a function of gate voltage. For 10  $\mu\text{m}$  channel devices at small values of  $|V_g - V_d|$ , the effective channel length decreased by a few  $\mu\text{m}$ , as determined by the position in the channel where the hole density had decreased by an order of magnitude compared to the density just outside the source.

The contact resistance was determined by plotting the total device resistance in the linear region as a function of the channel length. The total device resistance is given by the sum of the channel resistance (a linear function of channel length) and the contact resistance (a constant). Extrapolating

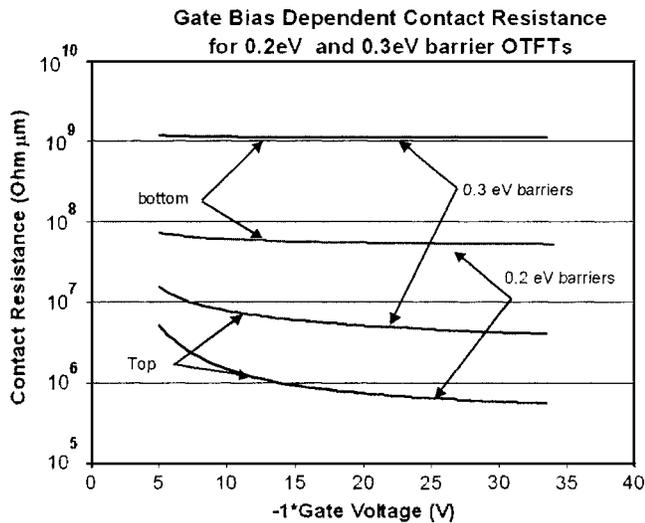


FIG. 3. Contact resistance for top and bottom contact devices with 0.2 and 0.3 eV source/drain hole injection barriers, as functions of the gate bias. The bottom contact devices were found to have a higher contact resistance than the top contact devices. The top contact resistances, however, demonstrate a much stronger gate bias dependence.

to a zero-length device gives the contact resistance. This was performed for each gate bias point in the linear region, giving the contact resistance as a function of gate bias. The results for top and bottom contact devices, with hole injection barriers of 0.2 and 0.3 eV are presented in Fig. 3. The following trends are noted: (1) the contact resistance for the 0.3 eV contacts are more than an order of magnitude larger than the 0.2 eV contacts, which is what one would qualitatively expect; (2) in each case, the contact resistance of the bottom contact devices appears to be approximately two orders of magnitude greater than the corresponding top contact device; and (3) while the contact resistance of the bottom contact devices appears to be almost independent of the gate bias, the top contact resistance is strongly dependent on the gate bias, increasing sharply at low gate-source voltage.

It is interesting to compare these results with the literature.<sup>2,3</sup> Necliudov *et al.* measured the contact resistance of Pd top and bottom contact pentacene OTFTs with measured mobilities of  $\sim 0.9 \text{ cm}^2/\text{V s}$ . The trends observed in

their study agree well with those observed in the simulations. For bottom contact devices, they measured a resistance of  $1.3 \times 10^8 \text{ Ohm } \mu\text{m}$ , consistent with an injection barrier of between 0.2 and 0.3 eV in the simulations. Additionally, they reported a top contact resistance that is strongly dependent on gate voltage, being much less than the bottom contact resistance at high gate bias, and increasing sharply at low gate bias.

The contact resistance measured experimentally has been shown to be consistent with simulations using reasonable parameters to describe the contacts. In particular, the difference between the top and bottom contact geometries has been accurately reproduced. It has also been demonstrated that short channel effects, such as channel length modulation must be taken into account when analyzing pentacene OTFT data from devices with channel lengths  $< 100 \mu\text{m}$ . Additionally, one must take into account that long channel devices, such as those typically studied in the laboratory, are relatively immune to high contact resistance, and that device performance may degrade when scaling to smaller channel lengths.

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