Influence of SiO_2 Dielectric Preparation on Interfacial Trap Density in Pentacene-Based Organic Thin-Film Transistors

J. W. H. Smith and I. G. Hill*
Department of Physics, Dalhousie University
Halifax, Nova Scotia B3H 3J5, Canada
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Organic thin-film transistors were fabricated using SiO_2 as the gate dielectric, and pentacene as the active layer. Two dielectric preparation methods, solvent cleaning and oxygen plasma cleaning, were used prior to pentacene deposition. The threshold voltage shifts and hysteresis of the saturation transfer characteristics were studied for a large number of devices, and statistically significant differences were identified. The threshold voltage shift between off-to-on and on-to-off sweeps was 13.2 $\pm$ 0.6V for solvent cleaned devices, and 4.4 $\pm$ 0.2 V for plasma cleaned devices. The improvement is attributed to the reduction in organic contamination at the semiconductor/dielectric interface following plasma cleaning, and a corresponding reduction in both hole and electron interfacial trapping states.

PACS numbers:

Introduction

Organic thin-film transistors (OTFTs) are a promising alternative technology to amorphous silicon devices. Free from traditional high temperature processing steps, they can be fabricated on a wide variety of low cost flexible substrates, including polyethylene terephthalate (PET) and naphthalate (PEN)[1]. The combination of low-temperature processing and flexible substrates may enable large-scale, low-cost, continuous manufacturing processes, resulting in a greatly reduced cost per unit area.

Pentacene OTFTs have been shown to have performance very similar to their amorphous silicon counterparts[2, 3] with carrier mobilities in the range of 1 cm^2/Vs and on-off ratios between 10^6 and 10^8. Major drawbacks of pentacene OTFTs, however, are their poor sub-threshold performance and typically large positive threshold voltages. Large sub-threshold slopes, on the order of about 5 volts/decade, and threshold voltages of a few tens of volts are typical of OTFTs having a SiO2 dielectric thickness of 350 nm.[4] These shortcomings have been addressed by the use of an several different self-assembled monolayers at the SiO2/pentacene interface, including octadecyltrichlorosilane (OTS)[2], hexamethyldisilazane (HMDS)[5, 6], and most recently 9-phosphonoanthracene[7]. It is generally accepted that the improved performance observed is the result of the elimination of charge trapping states at the semiconductor/dielectric interface. It has recently been suggested that electron-trapping hydroxyl groups are the cause of both the poor sub-threshold performance of polymer and molecular organic TFTs and the general absence of n-type conduction that has been observed in these devices[8]. The filled electron trap states prevent the Fermi level from moving within the semiconductor gap as the gate potential is changed. In the case of a p-type device with a large electron interfacial trap density, this resistance to Fermi level shifting results in a poor sub-threshold slope, but does not directly influence the observed hole mobility.

We present the results of a simple interface modification procedure: oxygen plasma cleaning of the SiO_2 surface prior to pentacene deposition. The purpose of this study is not to introduce another dielectric treatment procedure, but rather to study the effects and origins of the large densities of charge trapping states present at the bare SiO_2/pentacene interface. The electrical characteristics of devices fabricated using this procedure are compare to devices using only traditional organic solvent cleaning. Statistical analysis of a large number of devices of each type has revealed significantly different electrical properties. These differences have provided insight into the source and nature of the trapping states responsible for the large threshold voltage shifts and transfer characteristic hysteresis observed that depend on the direction of gate bias sweeps[9].

Experiment

Si(100) wafers (n-type, 0.001 Ωcm) with 100 nm of thermal SiO_2 were used as substrates. The heavily doped Si substrate and the SiO_2 served as a common gate and gate dielectric, respectively. The substrates were prepared using one of two procedures. First, a traditional solvent cleaning method was used in which the substrates were soaked in boiling trichloroethylene for 3 min, room temperature acetone for 3 min, and boiling methanol for 3 min. After removal from the boiling methanol, the samples were immediately blown dry using dry compressed air. In the second procedure, an oxygen plasma cleaning step was added after the cleaning in organic solvents. Oxygen plasma cleaning was performed in a parallel plate

*Electronic address: ian.hill@dal.ca

capacitive reactive ion etcher with 8 in diameter electrodes at 150 mTorr with an O_2 flow of 20 sccm for 4 min at a total delivered power of 25 W. Low etching power was used to gently clean the surface, avoiding damage to the dielectric. After removal from the reactor, the substrates were immediately loaded into the vacuum deposition system, minimizing their exposure to air.

Pentacene and gold were deposited by thermal deposition from resistively heated sources in a vacuum deposition system with a base pressure of $\approx 10^{-6}$ Torr. The pressure during deposition is $< 10^{-5}$ Torr. Pentacene crystals were purchased from America Organic Semiconductor, and were used without further purification. Pentacene was sublimed at 0.1-0.2 nm/s from a molybdenum boat with the substrate holder maintained at 70°C, as previously determined to be optimum in our system. 99.99% pure gold, purchased from Kurt J. Lesker, Co. was used for the source and drain contacts. Gold was evaporated from a tungsten wire basket filament at 0.2 nm/s with the sample nominally at room temperature.

Transistors were fabricated in the top contact geometry with gold source/drain contacts (50 nm) evaporated on top of the pentacene film (50 nm). Arrays of transistors were patterned by stencil masking of both the pentacene and gold layers. Patterning of the pentacene minimizes leakage currents and cross-talk between neighboring devices. The arrays contained transistors of three discrete channel widths (500 μm, 1000μm and 1500 μm) and four channel lengths (25 μm, 50μm, 100μm and 250 μm). These arrays produce transistors with a wide range of W/L ratios, from 2 to 60.

Transfer characteristics of the all devices were measured in both the saturation and linear modes of operation. This report will focus on the saturation transfer characteristics. Voltages were applied, and currents measured, by two Keithley 237 source-measure units with a current resolution of 10 fA. Source electrodes were held at ground potential. Drain electrodes were held at -25 V (saturation) or -1V (linear) with respect to the source (V_{DS}). The gate potential (V_{GS}) was swept from -25 V to +25 V for on-to-off sweeps, and from +25 V to -25 V for off-to-on sweeps. The saturation data were analyzed by plotting the square root of the drain current (I_D) as a function of gate voltage. The slope of a fit to the linear portion of this plot, above threshold, yields the field effect hole mobility, while the gate voltage intercept of the fit line determines the threshold voltage. The (inverse) subthreshold slope is determined by a linear fit to $\log(I_D)$ just as the current begins to increase. On-Off ratios were determined using the minimum observed drain current in the off region and the maximum current observed in the on region. On the order of 100 transistors each of solvent and plasma treated devices were analyzed in this study.

It was assumed that there exist very long-lived electron trapping states at the pentacene/SiO_2 interface that are populated when a large positive gate voltage is applied [9, 10]. Populating these traps will result in a large positive shift in the threshold voltage and a corresponding on-to-off/off-to-on hysteresis. Data were therefore taken in the following order: saturation on-to-off, saturation off-to-on, and linear. Thus, the saturation on-to-off sweep is the collected prior to any large positive voltage being applied to the gate, and therefore before populating the long-lived electron traps. In contrast, the off-to-on transfer characteristic is expected to be shifted by the influence of the now-populated traps. Thus, the hysteresis between the on-to-off and off-to-on will be used to study the density of interfacial charge trapping states.

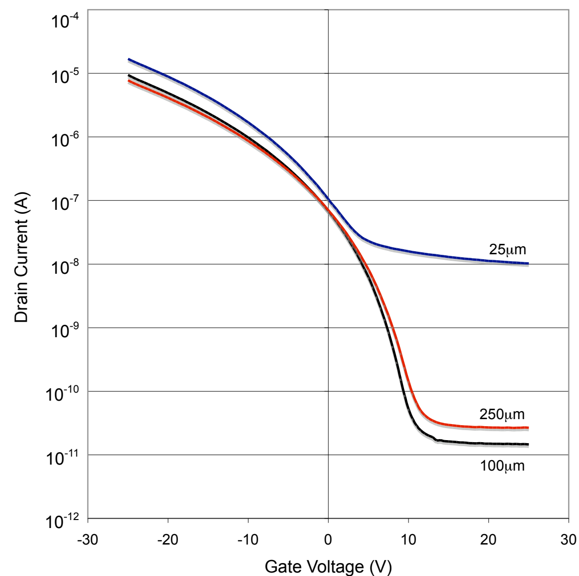

FIG. 1: Saturation transfer characteristics of devices of three different channel lengths fabricated on an oxygen plasma treated substrate. The poor sub-threshold behavior of the 25 μm devices is blamed on ill-defined stencil masked source-drain contacts. The currents have been normalized so that all three devices correspond to W/L ratios of 10.

Results

Figure 1 illustrates on-to-off saturation transfer curves for transistors with three different channel lengths (25 μm, 100 μm, and 250 μm) fabricated on an oxygen plasma treated substrate. As is evident in this figure, while the 100 μm and 250 μm curves look equivalent, within experimental uncertainty, the 25 μm curve suffers from a poor on-off ratio and worse sub-threshold performance, in general. In fact, the 25 μm device illustrated in Fig. 1 is one of the best performing devices of this channel length. Some showed little current modulation, with on-off ratios of $< 10^2$. This was evident of oxygen plasma treated and solvent cleaned substrates. We believe that this may be due to ill-defined source-drain contacts due to the stencil masking process. There may exist regions, defined as within the channel, which have significant amounts of source-drain metal contaminants,

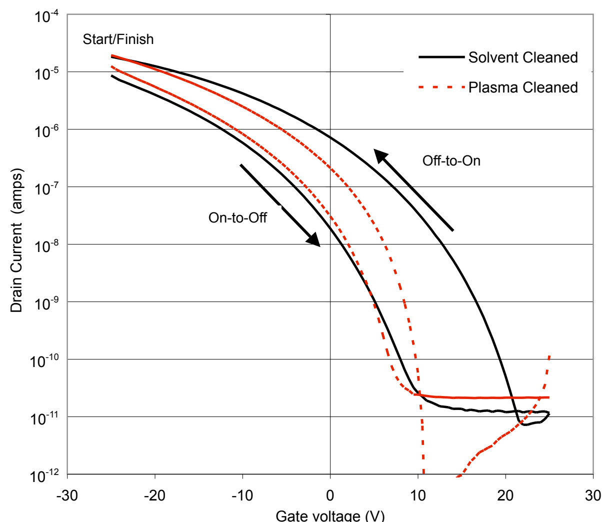

FIG. 2: Saturation transfer characteristics of an oxygen plasma treated device, and a solvent cleaned device. On-to-off, followed by off-to-on scans are presented, illustrating the magnitude of the hysteresis present in each case. Each device presented is characteristic of the average values of threshold voltage shifts observed.

which impact the function of the devices. The 50 μm devices were intermediate between the results of the 25 μm and 100/250 μm devices. For this reason, we chose to exclude the 25 μm and 50 μm devices from the discussion that follows.

We present on-to-off and off-to-on transfer curves (collected in that order) for typical oxygen plasma treated and solvent cleaned devices in fig. 2. A very large degree of hysteresis is evident in the solvent cleaned data, which manifests itself in a threshold voltage shift of 13.2 V between the two scans. A much smaller, but still significant, degree of hysteresis is present in the data collected from the oxygen plasma treated device, in which the threshold voltage shift was 4.5 eV. The same data is presented in figs. 3 and 4 for plasma treated and solvent cleaned devices, respectively. In these figures, the square root of the drain current is plotted as a function of the gate voltage. The hole mobility is extracted from the slope of the (near) linear portion of these plots, and the threshold voltage is defined as the voltage intercept of a fit to the linear portion. The threshold voltage shifts, described above, are clearly evident. closer examination of these figures reveals that while the slopes of the on-to-off and off-to-on sweeps of the plasma treated device are almost identical, the slope of the on-to-off sweep of the solvent cleaned device is steeper than the off-to-on sweep. This indicates a larger hole mobility for the solvent cleaned on-to-off sweep compared to the off-to-on. This trend was observed for all devices of each preparation, as will be presented below.

In order to examine whether or not the above trends were statistically significant, histograms showing the dis-

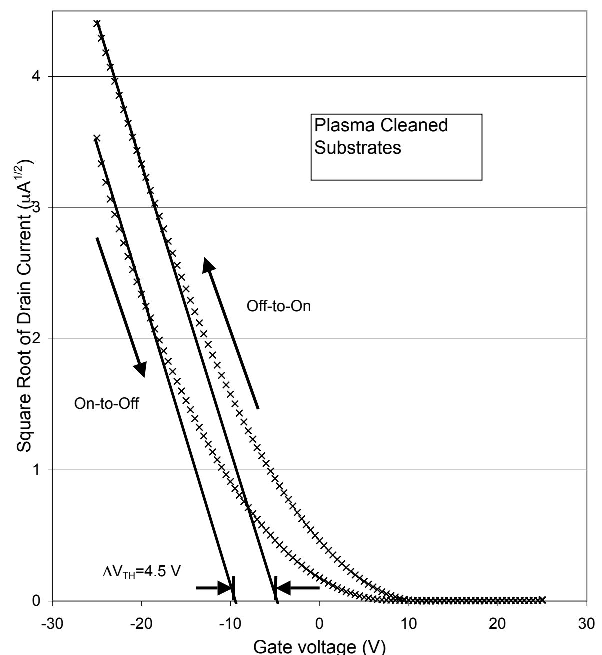

FIG. 3: Saturation transfer characteristics of an oxygen plasma treated device, with the square root of the drain current plotted as a function of gate bias. This is the same data as presented in fig.2. The threshold voltage shift of 4.5 V, and the equivalent slope between the two sweep directions is evident.

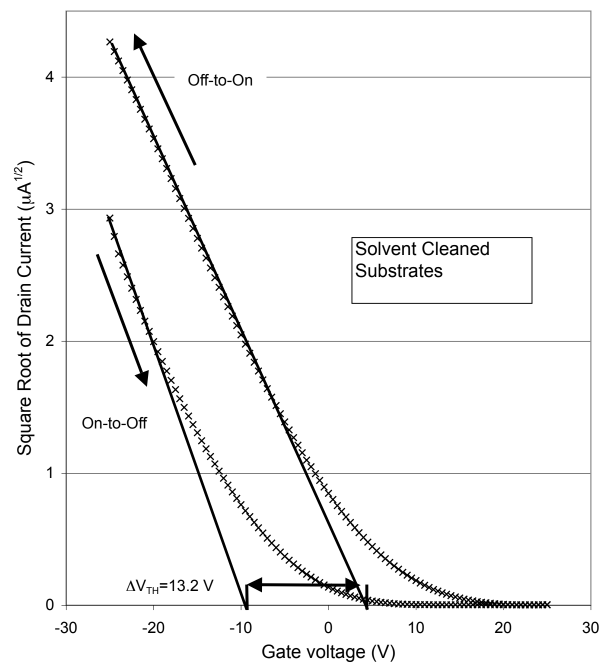

FIG. 4: Fig. 5: Saturation transfer characteristics of a solvent cleaned device, with the square root of the drain current plotted as a function of gate bias. This is the same data as presented in fig.2. The threshold voltage shift of 13.2 V, and the equivalent slope between the two sweep directions is evident.

tributions of threshold voltages and mobilities for each sweep direction and substrate preparation were constructed, as well as threshold voltage shifts between the sweep directions for each preparation. Data for the distribution of threshold voltages extracted from plasma treated devices is presented in fig. 5. In agreement with the earlier figures, we note that the threshold voltages of the off-to-on sweeps are shifted by ≈5 V with respect to the on-to-off sweeps. We also note that both distributions are clearly bimodal, which corresponds to the results obtained from two different substrates. It is evident that some difference in the preparation, perhaps a longer exposure to air prior to deposition of the pentacene, resulted in the substrate-to-substrate variation. If fig. 6 similar data are presented for the solvent-cleaned devices. Again, in agreement with the data presented in figs. 2-4, there is a clear shift of ≈ 14V of the off-to-on threshold voltages compared to the on-to-off. It is also noted that the solvent cleaned on-to-off threshold voltages are ≈ 5V more *negative* than those of the plasma treated on-to-off sweeps. Similarly, the solvent cleaned off-to-on threshold voltages are ≈ 5V more *positive* than those of the plasma treated on-to-off sweeps. The threshold voltage shifts, defined as the off-to-on threshold minus the on-to-off threshold, calculated for each device, are presented as a histogram in fig. 7. We note that these shifts are positive in all cases, that the magnitude of the shift is much larger for solvent cleaned devices than for plasma cleaned devices, and that the width of the distribution is much larger for the solvent cleaned devices.

The statistical distributions of the hole mobilities are presented in figs. 8 and 9 for plasma and solvent cleaned devices, respectively. Confirming the qualitative observations of the slopes observed in figs. 3 and 4, we note that while distributions of mobilities in the on-to-off and off-to-on sweep directions for plasma cleaned devices overlap, with only a small shift to larger mobilities in the on-to-off direction, a large shift of ≈ 0.2 cm^2/Vs is observed for the solvent cleaned devices. In fact, the average mobility is almost twice as large in these devices during the on-to-off sweep compared to the off-to-on sweep.

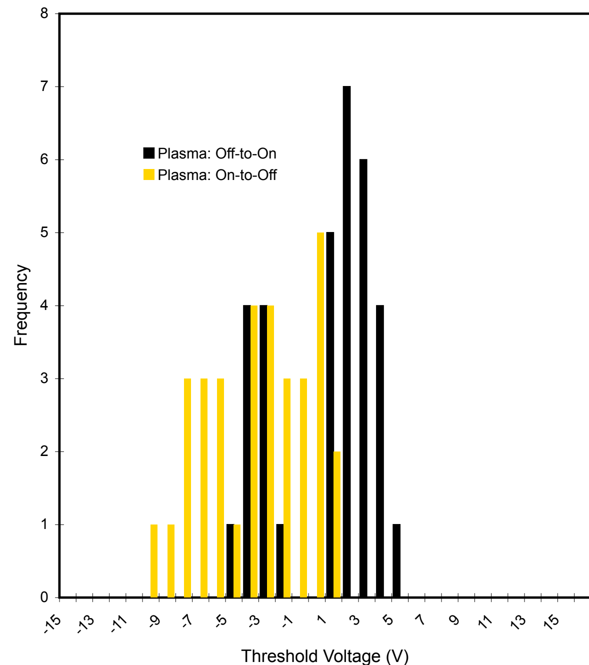

FIG. 5: Distribution of threshold voltages for plasma treated devices in the on-to-off and off-to-on sweep directions. Note that each distribution is bimodal, corresponding to two different substrates.

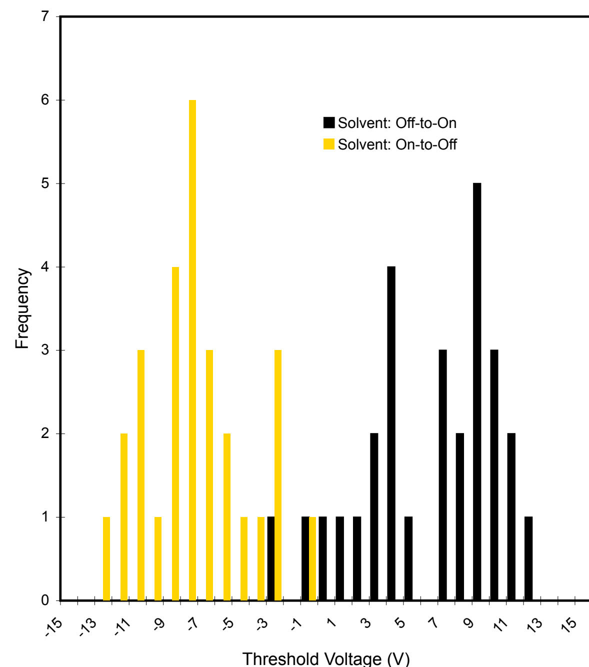

FIG. 6: Distribution of threshold voltages for solvent cleaned devices in the on-to-off and off-to-on sweep directions.

Discussion

A summary of the statistical data presented in the preceding section is included in table I. In addition, data for the subthreshold slopes has been included. The subthreshold slopes are typical for pentacene devices fabricated on 100 nm SiO_2 dielectrics but are much poorer that those fabricated on SAM-treated SiO_2 [2, 3, 7], indicating a large density of charge-trapping states at the semiconductor/gate dielectric interface. This conclusion is supported by the large threshold voltage shifts and corresponding hysteresis observed.

Following Bolognesis et al [10], we interpret the observed threshold shifts in the following way. If a large density of electron trapping states, for instance, are

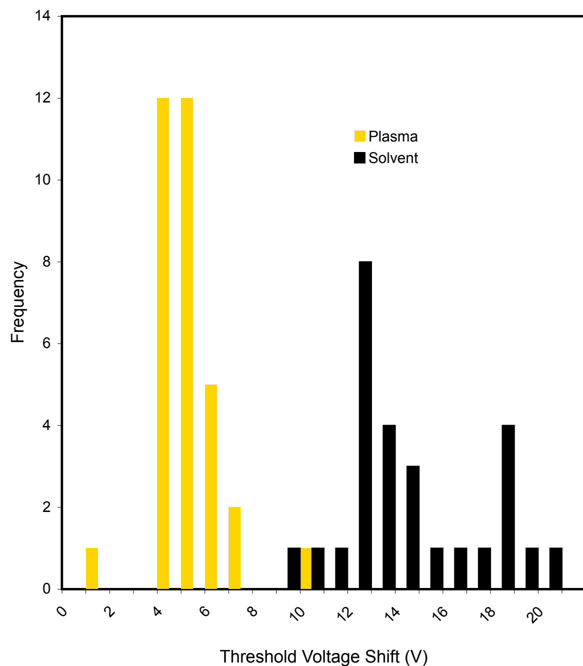

FIG. 7: Distribution of threshold shifts between the two sweep directions for plasma and solvent cleaned devices. The shifts are positive in all cases.

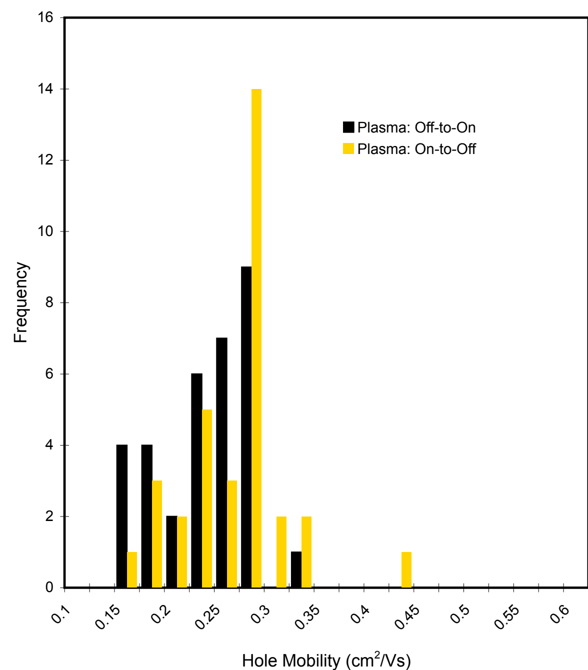

FIG. 8: Distribution of hole mobilities extracted from the on-to-off and off-to-on sweeps for plasma treated devices.

TABLE I: Comparison of parameters, uncertainties and statistics extracted from the study of 100 μm and 250 μm channel length devices

	On-to-Off		Off-to-On	
	Mean	σ	Mean	σ
	Plasma Cleaned Substrates			
μ_h (cm^2/Vs)	0.26±0.01	0.05	0.22±0.01	0.05
S (V/decade)	2.7 ± 0.1	0.6	1.6 ± 0.1	0.7
V_{th} (V)	-4.2±0.5	3.1	0.2±0.5	3.0
ΔV_{th}(V)	4.4 ± 0.2, σ=3.3			
	Solvent Cleaned Substrates			
μ_h (cm^2/Vs)	0.41±0.04	0.18	0.21±0.01	0.08
S (V/decade)	2.6 ± 0.1	0.7	2.0 ± 0.2	1.1
V_{th} (V)	-8.2±0.6	3.1	5.6±0.8	4.1
ΔV_{th}(V)	13.8 ± 0.6, σ=3.3			

present at the semiconductor/dielectric interface, the application of a large positive gate bias will tend to populate these states, and when the gate bias is then swept in the negative direction, turning the p-type device on, the long-lived electron trap states will remain populated, shifting the threshold voltage by an amount ΔV_{th}=-q_{trap}/C_{ox}, where q_{trap} is the areal density of trapped charge, and C_{ox} is the capacitance/area of the gate dielectric. Another way of viewing this phenomenon [9] is that at a given gate bias above threshold, the *net* charge in the channel region must be given by the $q_{net}=C_{ox}V_{gs}$. If there is negative charge present due to the trapped electrons, then there must be a correspondingly higher density of holes present, which increases the observed drain current for a given gate bias, effectively shifting the entire transfer curve to more positive gate bias.

Continuing with this interpretation, we note that if all of the observed threshold voltage shifts and hysteresis were due to the trapping of electrons at the interface, we would not expect to see the larger *negative* threshold voltages observed for the solvent cleaned on-to-off sweeps, compared to the same sweeps of the plasma cleaned devices. This would seem to indicate that there are also long-lived hole trapping states at the interface.

The reduction in the magnitude of the hysteresis observe for plasma cleaned devices can be understood if we attribute the origin of at least some of these charge trapping states to residual organic molecules on the SiO_2 surface, which are unavoidable for any substrate which is exposed to air. In particular, it is reasonable to assume that a such a layer will be present following cleaning in the organic solvents. Oxygen plasma cleaning is very efficient at removing organic residue from the surface, and is widely used in the semiconductor industry to remove organic contaminants and to strip organic-based oxides during wafer processing. We therefore propose that our oxygen plasma cleaned samples contain a lesser quantity of organic contaminants than do the solvent cleaned samples. Some contamination is unavoidable, as the samples are exposed to air between plasma cleaning and subsequent pentacene deposition. This scenario is consistent with the magnitudes of the observed threshold voltage shifts. It does not, however, explain the significantly higher hole mobilities observed in the on-to-off sweep di-

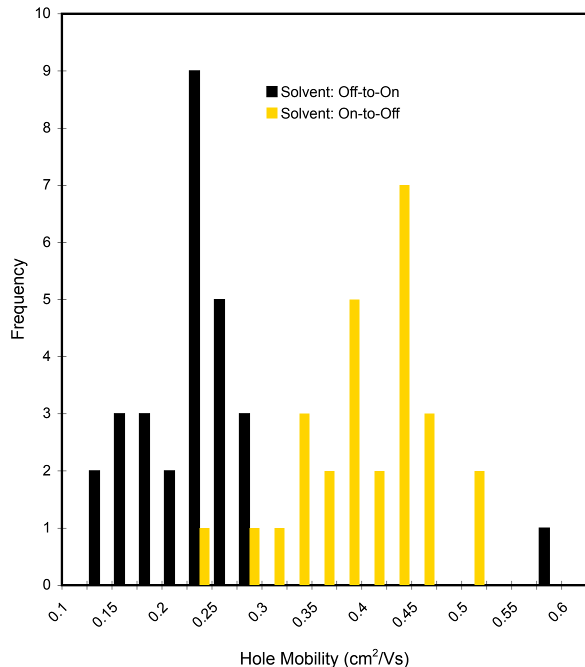

FIG. 9: Distribution of hole mobilities extracted from the on-to-off and off-to-on sweeps for plasma treated devices.

rection in the solvent cleaned data. It is possible that while the organic contaminants do result in charge trapping states at the interface, they may also provide a surface more suitable for pentacene growth, resulting in a improved film crystallinity and better intrinsic mobility. This increased mobility may be somewhat suppressed by a Coulombic interaction with the charged electron traps in the off-to-on state, resulting in the lower observed mobility. This is just speculation, but AFM studies of pentacene growth on the solvent and plasma cleaned surfaces may help to support or disprove this conjecture.

Conclusions

By studying a large number of pentacene OTFTs fabricated using both solvent and oxygen plasma cleaned SiO_2 gate dielectrics we have identified statistically significant differences in the threshold voltages, threshold voltage shifts, and transfer characteristic hysteresis when the gate bias is cycled between the on and off states of the transistors. We have attributed the observed shifts to the presence of long-lived hole and electron traps at the pentacene/SiO_2 interface, at least some of which are the result of organic contaminants on the surface prior to pentacene deposition. Oxygen plasma cleaning greatly reduces, but does not eliminate, these effects. Interestingly, significantly larger hole mobilities were observed on solvent cleaned substrates in the on-to-off sweep direction, but these were suppressed when the gate bias was cycled from off-to-on.

Acknowledgments

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