Influence of Channel Stoichiometry on Zinc Indium Oxide Thin-Film Transistor Performance

Matthew G. McDowell and Ian G. Hill

***Abstract*—Thin-film transistors using a semiconductor of the form $(ZnO)_x(In_2O_3)_{1-x}$ were fabricated via combinatorial RF sputtering. Stoichiometries varied from $x = 0.5$ to $x = 1$. Two sets of devices were annealed under oxygen at 300 °C and 600 °C, with another left as deposited. Devices fabricated with a zinc oxide fraction of 0.67 ± 0.02 were found to exhibit the highest mobilities of 35 $cm^2/V \cdot s$ for 300 °C annealing conditions. Peak performance was found for $x = 0.75 \pm 0.02$, which yielded near-zero turn-on voltages, inverse subthreshold slopes of 0.3 V/dec, and on/off ratios up to 10^9.**

***Index Terms*—Amorphous oxide semiconductors, combinatorial sputtering, RF magnetron sputtering, thin film transistors.**

I. Introduction

A GREAT deal of attention is being given to amorphous semiconductor devices and fabrication techniques that allow the use of low-cost large-area substrates for use primarily in displays. Current commercial large-area devices use amorphous silicon (a-Si), most commonly in LCD panels. Additional research is focusing on the use of organic semiconductors such as pentacene [1], [2]. However, both organic and a-Si semiconductors are limited to field-effect mobilities of ∼1 $cm^2/V \cdot s$. Recent research into semiconductors composed of metal oxides [3], [4] and combinations of oxides [5]–[7] has yielded results with mobilities as high as 50 $cm^2/V \cdot s$ along with excellent on/off ratios. A number of these semiconductors have the added benefit of being transparent, making them ideally suited for use in both conventional and heads-up displays. In particular, zinc indium oxide (ZIO) shows promise as a high-mobility transparent semiconductor. Research on this material has focused on two regimes: one of indium-rich devices [8]–[10] and another of zinc-rich devices [11]–[14]. We have chosen to focus on the latter. While a great deal of work has been done to study structure [15], RF characteristics [14], and charge transport [16] in ZIO films, devices have only been fabricated for a small number of discrete molar ratios, due to the difficulties involved in preparing sputtering targets for individual stoichiometric ratios of interest. In the zinc-rich regime, the most successful of these was 2:1 $(ZnO : In_2O_3)$, annealed at temperatures of 300 °C and 600 °C yielding field-effect mobilities of ∼20 and ∼50 $cm^2/V \cdot s$, respectively [11]. Our experiment seeks to study transistor performance as a function of stoichiometry for zinc-rich ZIO devices by employing a combinatorial fabrication technique that allows the characterization of devices for a large number of different stoichiometries. While prior combinatorial work has been done for similar devices composed of indium, zinc, and gallium oxides [17], the gallium content in these devices was never less than 10%, and therefore, the pure ZIO range of stoichiometries has not yet been explored.

II. Experiment

The devices in this experiment were of a top-contact design, with substrates of heavily doped silicon (n-type, arsenic, $< 0.005\ \Omega \cdot cm$) with 1000 ± 20 Å thermally grown SiO_2, acquired from Silicon Quest International. The doped silicon was used as the gate, with the SiO_2 acting as the dielectric. Prior to sputtering, each wafer was oxygen-plasma cleaned at a power density of 0.08 W/cm^2 at a pressure of 150 mTorr for 4 min.

The combinatorial RF sputtering technique used yielded a thin film that varied linearly and continuously from one stoichiometry to another. Two 50-mm sputter targets were used, one of ZnO (99.999%) at a power of 40 W and the other of In_2O_3 (99.99%) at 90 W, both purchased from Kurt J. Lesker Co. A preliminary study found films sputtered under 10% O_2 and 90% Ar to be highly conductive, and another work [18] has shown the conductivity of sputtered ZIO films to be highly sensitive to the oxygen content of the sputter gas, probably as a result of doping due to oxygen vacancies in the resulting film. Therefore, sputtering took place in 20% oxygen and 80% argon, at a total pressure of 5 mTorr. To achieve the combinatorial range of stoichiometries, the targets were placed at a fixed distance from the center of a chamber containing a rotating table to which the substrates were affixed. In initial studies, the sources were masked such that the amount of ZnO deposited rose linearly from the inner to the outer edge of the sputtering "track," while In_2O_3 deposition increased from the outer to the inner edge. This resulted in a film of the form $(ZnO)_x(In_2O_3)_{1-x}$, varying linearly from $x = 0$ to $x = 1$. However, in later studies, the sources were masked such that the amount of ZnO deposited was constant for all radii within the track, and In_2O_3 was sputtered such that the amount deposited varied linearly from a molar amount equal to ZnO at the inner edge of the track to zero at the outer edge, resulting in a film varying from $x = 0.5$ to $x = 1$. A maximum of 0.2 Å of material was deposited on each rotation,

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ensuring intimate mixing of the two oxides, for a total film thickness of 800 Å at the inner edge of the track to 400 Å at the outer edge. This film thickness was verified after deposition using a Dektak profilometer. Further details of this technique are given elsewhere [19]. The table was water cooled such that the substrates were held at ∼12 °C during sputtering. The ZIO on each wafer was patterned using a stainless steel stencil mask during sputtering to ensure that the semiconductor for each device would be electrically isolated from its neighbors. To reduce unintentional doping due to oxygen vacancies, the wafers were annealed under oxygen for 1 h at either 300 °C or 600 °C or left as deposited.

The stoichiometry of the films was determined using a JEOL JXA-8200 Electron Probe Microanalyzer in WDS mode on an as-deposited wafer. Our studies have shown that the atomic ratio of zinc to indium as a function of position is not affected by annealing. Using the detection geometry and measured film mass and thickness data, Casino (v2.42) was used to model differences in the interaction volumes for the production of L_α X-rays from indium and zinc. Due to the limited thickness of the films, the results of this modeling were needed to make corrections to the Zn:In ratios derived from the WDS data. Stoichiometry (expressed as $(\mathrm{ZnO})_x(\mathrm{In_2O_3})_{1-x}$) was found to vary linearly from $x = 0.55$ to $x = 1.0$ across the sample. The crystalline structure of the oxide under each annealing condition was examined with glancing angle X-ray diffraction using a curved multiangle detector (∼6° incident angle using Cu $\mathrm{K}_{\alpha 1,\alpha 2}$ X-rays). Additionally, transparency was examined for films on glass using an Ocean Optics USB2000 spectrometer and an incandescent light source. Transparency was defined as the ratio of transmitted light through the glass/film system to transmitted light with no glass or film. No corrections were made for reflections at the interfaces.

Aluminum source and drain contacts were patterned via thermal deposition through stainless steel stencil masks, for a total of 256 devices per wafer. W/L ratios varied between 16 and 4, with channel lengths of 125–500 μm.

III. Results and Discussion

The resulting n-type devices were tested by taking both linear and saturation transfer curves in atmosphere and under room lighting using two Keithley 237 source–measure units. The source–drain current was recorded while sweeping the gate–source voltage from +25 (on) to −25 V (off) and back again, while the drain–source voltage was held at +0.1 V for linear curves and +25 V for saturation curves. A single gate contact was made by scratching through the $\mathrm{SiO_2}$ to the doped silicon substrate. Field-effect mobility was determined using the ideal transistor equations

$$K = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L} \tag{1}$$

$$i_{\mathrm{DS}}^{\mathrm{sat}} = K(V_{\mathrm{GS}} - V_T)^2, \qquad V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_T \tag{2}$$

$$i_{\mathrm{DS}}^{\mathrm{lin}} = 2K(V_{\mathrm{GS}} - V_T)V_{\mathrm{DS}} - V_{\mathrm{DS}}^2, \qquad V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_T. \tag{3}$$

Here, $i_{\mathrm{DS}}^{\mathrm{lin}}$ and $i_{\mathrm{DS}}^{\mathrm{sat}}$ are the linear and saturation mode source–drain currents, respectively, μ is the electron mobility,

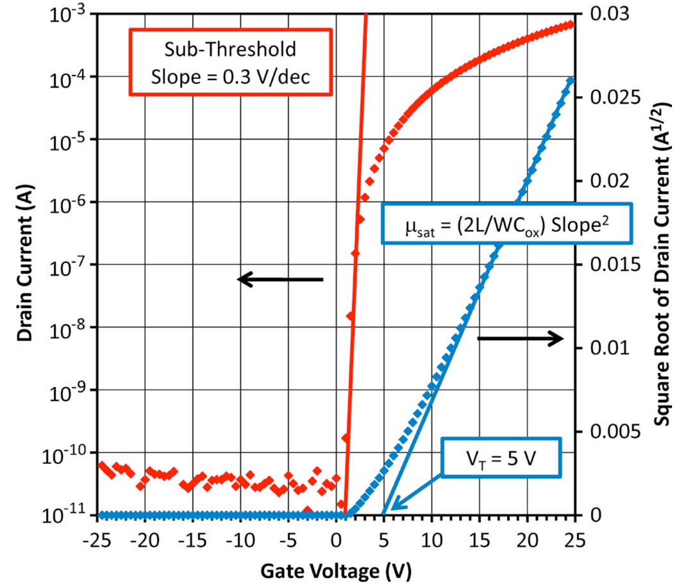

Fig. 1. Typical saturation transfer curve with $V_{\mathrm{DS}} = +25$ V. This figure shows the methods used to determine saturation mobility, threshold voltage, and subthreshold slope. The device has a channel stoichiometry corresponding to $x = 0.74$.

W/L is the ratio of the channel width to length, C_{ox} is the capacitance of the $\mathrm{SiO_2}$, V_{DS} is the drain–source voltage, V_{GS} is the gate–source voltage, and V_T is the threshold voltage. Saturation mobility was determined using the slope of the square root of the source–drain current and linear mobility using the slope of the source–drain current, both as a function of gate voltage. Threshold voltages were determined by finding the voltage axis intercept of these regions (see Fig. 1). Subthreshold slopes were found by taking the maximum slope of $\log(i_{\mathrm{DS}})$ versus V_{GS} in the subthreshold region. On/off ratios were taken as the ratio of the maximum to minimum observed source–drain current.

A typical saturation transfer curve for a device annealed at 300 °C is shown in Fig. 1. Using these curves, devices annealed at 300 °C and 600 °C were found to exhibit saturation mobilities of up to 40 and 20 $\mathrm{cm^2/V \cdot s}$, respectively (Fig. 2). Linear mobilities were similar to saturation mobilities for 300 °C annealed films, but were up to 30 $\mathrm{cm^2/V \cdot s}$ for films annealed at 600 °C, likely due to a reduced effect contact resistance between the annealed film and the aluminum contacts during linear mode testing. On/off ratios for $x > 0.6$ varied between 10^6 and 10^9 and are highest for $0.6 < x < 0.75$. Below $x = 0.6$, on/off ratios fell dramatically (to as low as 10), making mobilities impossible to determine using the ideal transistor equations. All devices exhibited an upward trend in mobility with increasing $\mathrm{In_2O_3}$ content for $x > 0.60$, with peak mobilities at a zinc oxide fraction of 0.67 ± 0.02 for 300 °C devices and 0.60 for 600 °C. However, inverse subthreshold slopes reached a minimum of 0.3 and 0.5 V/dec (for 300 and 600 °C), turn-on voltages (taken to be the voltage at which an exponential increase in source–drain current is observed) were near 0 V, and threshold voltages were ∼5 V for $x = 0.75 \pm 0.02$, while mobilities at this ratio are only 10%–20% below the highest mobilities. It can therefore be argued that devices at this ratio of 3 : 1 ZnO:$\mathrm{In_2O_3}$ exhibit "peak performance." Inverse

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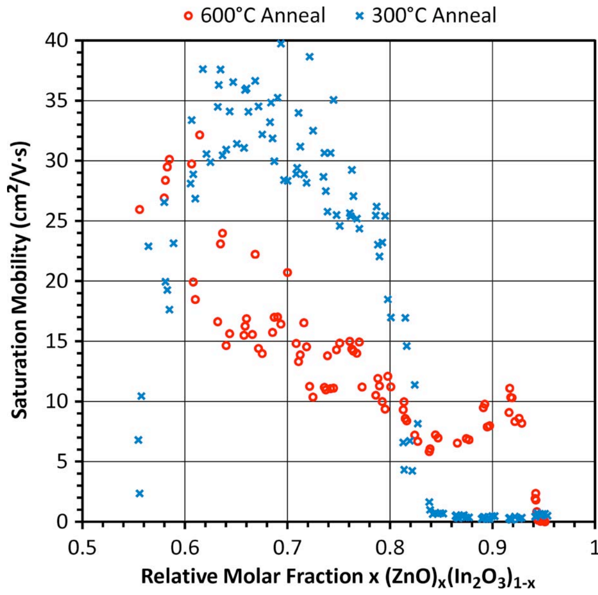

Fig. 2. Mobility as a function of channel stoichiometry for both 300 °C and 600 °C annealing conditions.

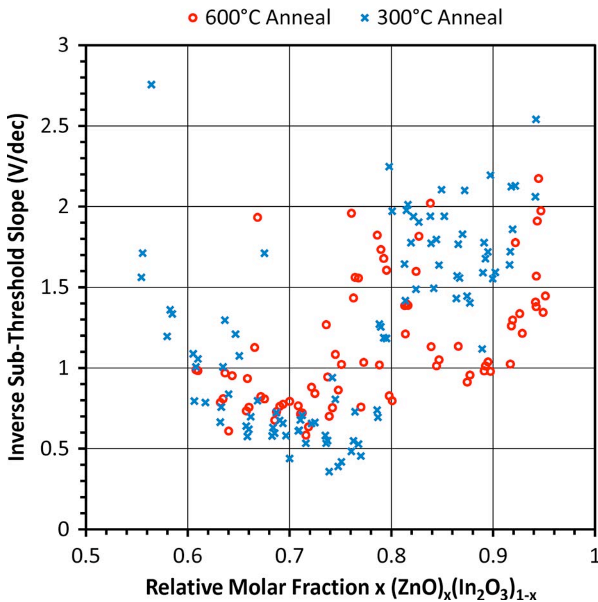

Fig. 3. Subthreshold slopes for 300 °C and 600 °C annealing conditions as functions of molar ratio.

subthreshold slopes were found to be strongly dependent on both the stoichiometry and annealing conditions (Fig. 3). During testing, no significant hysteresis was observed between the on–off and off–on sweeps. Devices using as-deposited films were found to be insulating with drain currents on the order of 10^{-10} A for all gate voltages in the sweep, independent of stoichiometry. Mobility was found to be independent of W/L (4, 4/3, 8, 16) within the experimental scatter of $\sim$10% at a given stoichiometry. Other work [8], [20] has shown a relationship between ZIO semiconductor thickness (from 15 to 60 nm) and mobility. This relationship was very pronounced at the thin end of their tested range, but mobility did not appear to change significantly over the range tested here (40–80 nm), and no relationship between performance and thickness was

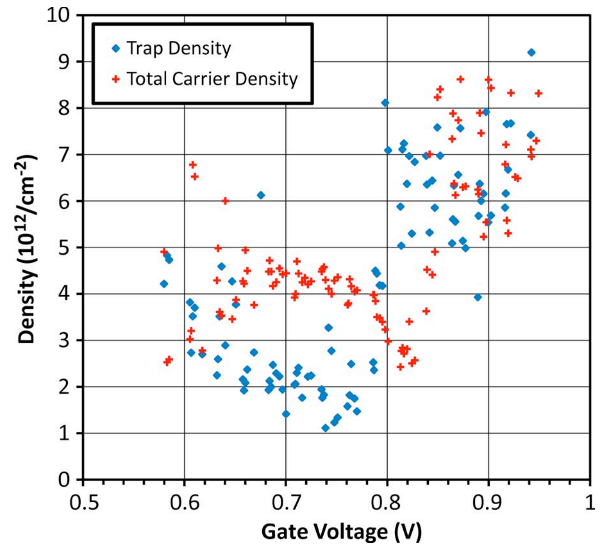

Fig. 4. Carrier and charge-trap densities for the 300 °C sample set. Note the abrupt drop in trap density around $x = 0.80$ that coincides with the reported trend in mobility (Fig. 2).

apparent in our devices. Devices were tested in air over a period of several days, during which time no change in behavior due to atmospheric exposure was observed. However, a single set of devices was briefly re-examined after approximately seven months of storage in air. This set showed significant reductions in both mobility (on the order of 10%) and threshold voltage (~ -10 V). The source of this change is not currently understood.

The 300 °C annealed devices exhibited a very sudden change in mobility around $x = 0.80$, with mobility approximately two orders of magnitude higher for lower ZnO concentrations. This abrupt increase in mobility is accompanied by a decrease in the inverse subthreshold slope. Using these subthreshold slopes and the threshold voltages determined from the saturation transfer characteristics, both the trap and charge carrier densities can be determined for devices in this region. An upper bound on the charge trap density was found using [21]

$$N_{\text{trap}} = \left(\frac{qS\log(e)}{kT} - 1\right)\frac{C_{\text{ox}}}{q} \times 1\ \text{eV} \quad (4)$$

assuming the traps to be uniformly distributed over an energy on the order of 1 eV below the conduction band edge. The charge density was determined using

$$N_{\text{charge}} = (V_{\text{GS}} - V_T)\frac{C_{\text{ox}}}{q}. \quad (5)$$

Here, S is the inverse subthreshold slope, q is the charge per carrier, and C_{ox} is the capacitance per unit area of the device dielectric (Fig. 4). In the range of stoichiometries above 80% ZnO, the trap density is approximately equal to the charge density. Therefore, almost all charges in the channel are trapped, resulting in apparent mobilities close to zero. For $x < 0.80$, the trap density falls to approximately half of the total induced charge density, and the average mobility rises to 35 $\text{cm}^2/\text{V}\cdot\text{s}$ at the peak performance stoichiometry. Since the method used to derive this value yields the average mobility of charge

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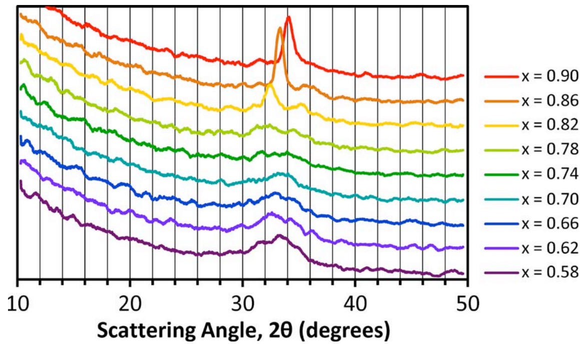

Fig. 5. XRD example data for 600 °C annealing conditions at a variety of film stoichiometries. It should be noted that XRD data was taken for different stoichiometries in steps of $\delta x = 0.02$. For clarity, only selected stoichiometries are shown.

carriers in the channel, we note that the mobile nontrapped charges in the channel may therefore have mobilities close to 70 $\mathrm{cm^2/V \cdot s}$, nearing the high mobilities reported for indium-rich devices [8].

A glancing-angle XRD (Fig. 5) showed a sharp peak at $2\theta = 34^\circ$ for $x = 0.86$ for films annealed at 600 °C, but no peak is visible for the 300 °C films. The intensity of the sharp peak decreased with increasing In_2O_3 content and was no longer visible for $x < 0.82$. The angle of the peak also decreased to 32° at a stoichiometry of $x = 0.82$. This crystalline phase appears to have a significant positive impact on transistor performance; where $x > 0.82$, devices made under the 600 °C annealing conditions were found to have mobilities of 10 $\mathrm{cm^2/V \cdot s}$, threshold voltages of ∼8 V, and subthreshold slopes of 1 V/dec, while films annealed at 300 °C at these stoichiometries yielded only 0.5 $\mathrm{cm^2/V \cdot s}$, with threshold voltages between −5 and −15 V and inverse subthreshold slopes of 1.5 V/dec. However, all annealing conditions showed only a very broad peak from 31° to 36° for $x < 0.82$. This broad peak is consistent with the work of Dehuff *et al.* [11] for low annealing temperatures, but our films were not observed to crystallize under high temperature annealing, even at 700 °C. This may be due to differences in annealing conditions or relative uncertainties in annealing temperature.

At high ZnO concentrations, the films were found to be between 80% and 90% transparent in the visible, with higher transparency in the red than in the blue. Films become more transparent in the blue with increasing In_2O_3 content for $x < 0.65$.

IV. Conclusion

ZIO $((\mathrm{ZnO})_x(\mathrm{In_2O_3})_{1-x})$ thin-film transistors have been fabricated for $0.5 \leq x \leq 1$. Peak-performing transistors were found to be those fabricated using an amorphous film of molar ratio $x = 0.75$ when annealed under oxygen at 300 °C. The devices exhibited mobilities of up to 40 $\mathrm{cm^2/V \cdot s}$, inverse subthreshold slopes as low as 0.3 V/dec, on/off ratios as high as 10^9, and near-zero threshold voltages. Devices with molar ratios < 0.80 were found to have charge trap densities comparable to the total gate-field-induced density when annealed at 300 °C and, therefore, very low average mobilities. Crystallization occurs in the same range when annealed at 600 °C, resulting in an decreased trap density and an order of magnitude increase in average mobility. Even the best performing devices, at a molar ratio of ≈ 0.75, have a sizable fraction of the total charge occupying trap sites, resulting in measured average mobilities that are most likely significantly lower than the free carrier mobility. A better understanding of the origin of these trap states may lead to methods of trap elimination, such as the passivation of dangling bond states as in hydrogenated amorphous silicon.

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